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Our Docket No.: 42390P17251

*Utility Patent Application*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Patent Application of:

Tatiana Shpeisman

Serial No.: 10/748,384

Examiner: Wei, Zhang

Assignee: Intel Corporation

Filed: December 29, 2003

Art Unit: 2194

For: Data Layout Mechanism To Reduce  
Hardware Resource Conflicts

**SUPPLEMENTAL RESPONSE TO OFFICE ACTION**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that I am causing the above-referenced correspondence to be delivered to the USPTO via facsimile transmission to (703) 872-9306 and that this paper or fee has been addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: February 21, 2007  
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Signature

February 21, 2007  
Date

Docket No.: 42390P17251  
Application No.: 10/748,384

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**INTRODUCTORY COMMENTS**

Sir:

This submission is intended to supplement the Response to Office Action filed December 21, 2006 (filed in response to the Office Action dated September 14, 2006, hereinafter "the previous Office Action"). A revised IDS accompanies this Supplemental Response. Applicant respectfully requests the Examiner to consider the following Remarks.

**No amendments are made by this supplemental response.**

**Remarks begin on page 3 of this paper.**